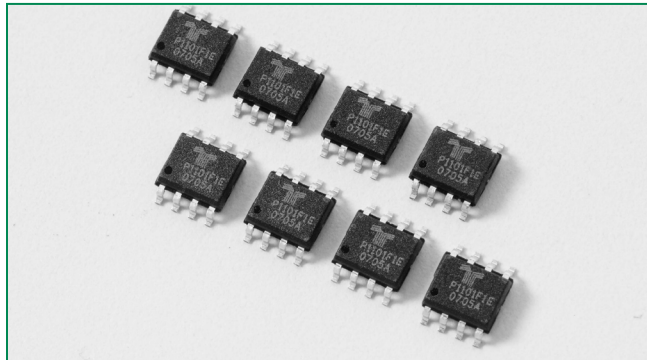


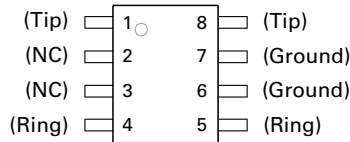
Fixed Voltage Enhanced Single Port Series - MS-012



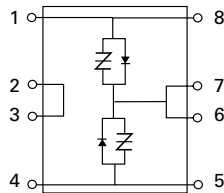
Agency Approvals

Agency	Agency File Number
	E133083

Pinout



Schematic Symbol



Description

The MS-012 packaged Fixed Voltage Enhanced Single Port Series are SIDACtor® components designed to protect sensitive SLICs (Subscriber Line Interface Circuit) from damaging overvoltage transients.

The series provides single port protection using a fixed voltage switching device for negative surges. Positive surges are routed through enhanced switching diodes to a ground reference. The series is also pin-to-pin compatible to industry standard programmable SO-8 SLIC protectors.

Features & Benefits

- Integrated fast switching diodes for positive voltage surges
- RoHS Compliant and Lead-Free
- Single port protection in one package
- Low voltage overshoot
- Low on-state voltage
- Pin-to-pin SO-8 compatible footprint
- Fails short circuit when surged in excess of ratings
- Does not degrade surge capability after multiple surge events within limit
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21 Enhanced Level
- ITU K.20/21 Basic Level
- GR 1089 Intra-building*
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

* Series resistance required

Electrical Characteristics

Part Number	Marking	$V_{DRM}@I_{DRM}=5\mu A$	$V_S@100V/\mu s$	I_H	I_S	$I_T@V_T$	$V_T@I_T=1$ Amps	$V_F@25^\circ$	Capacitance
		V min	V max	mA min	mA max	A max	V max	V max	
P0641DF-1E	P0641F1E	58	77	150	800	1	5	5	See Capacitance Values Table
P0721DF-1E	P0721F1E	65	88	150	800	1	5	5	
P0901DF-1E	P0901F1E	75	98	150	800	1	5	5	
P0991DF-1E	P0991F1E	80	104	150	800	1	5	5	
P1001DF-1E	P1001F1E	85	110	150	800	1	5	5	
P1101DF-1E	P1101F1E	95	130	150	800	1	5	5	
P1301DF-1E	P1301F1E	120	160	150	800	1	5	5	
P1701DF-1E	P1701F1E	160	200	150	800	1	5	5	

Notes:

- Absolute maximum ratings measured at $T_A=25^\circ C$ (unless otherwise noted).
- Components are not appropriate for positive ringing systems
- All electrical characteristics shown are defined from Tip (pins 1 & 8) to Ground (pins 6 & 7), and Ring (pins 4 & 5) to ground (pins 6 & 7)
- $V_F < 8.5$ volts @ 10 / 700µs, 375 Amps

Capacitance Values

Part Number	pF Pin 1,8-6,7 / 4,5-6,7 Tip-Ground, Ring-Ground		pF Pin 1,8-4,5 Tip-Ring	
	MIN	MAX	MIN	MAX
P0641DF-1E	40	90	20	45
P0721DF-1E	35	85	20	45
P0901DF-1E	30	80	20	40
P0991DF-1E	25	75	15	35
P1001DF-1E	25	75	15	35
P1101DF-1E	25	70	15	30
P1301DF-1E	20	70	15	30
P1701DF-1E	20	70	15	30

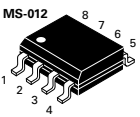
Note: Off-state capacitance (C_o) is measured at 1 MHz with a 2V bias

Surge Ratings

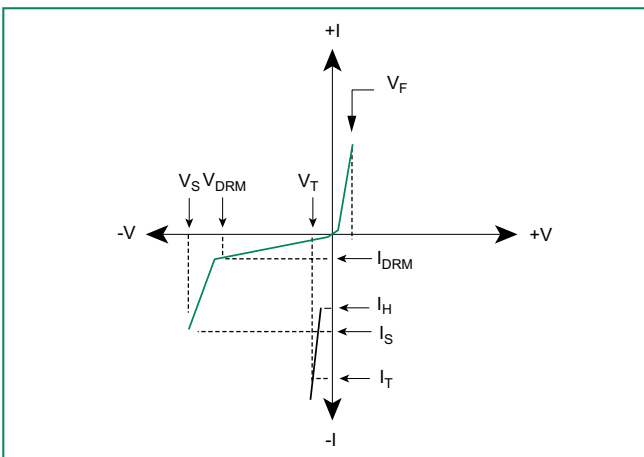
Series	I_{PP}				I_{TSM}	di/dt
	2/10 μ s	1.2/50 μ s/8/20 μ s	10/700/5/310 μ s	10/1000 μ s	600V _{RMS} 1s	
F	A min	A min	A min	A min	A min	Amps/ μ s max
	120	100	50	30	1	500

- Notes:
- Peak pulse current rating (IPP) is repetitive and guaranteed for the life of the product that is in thermal equilibrium.
 - I_{pp} ratings applicable over temperature range of -40°C to +85°C
 - The component must initially be in thermal equilibrium with -40°C $\leq T_J \leq$ +150°C

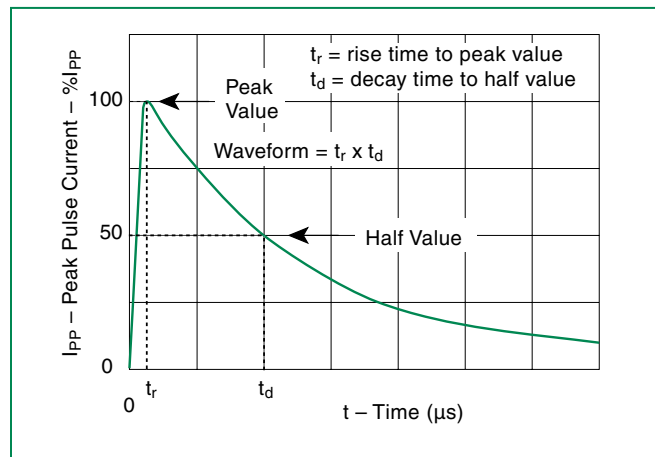
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	120	°C/W

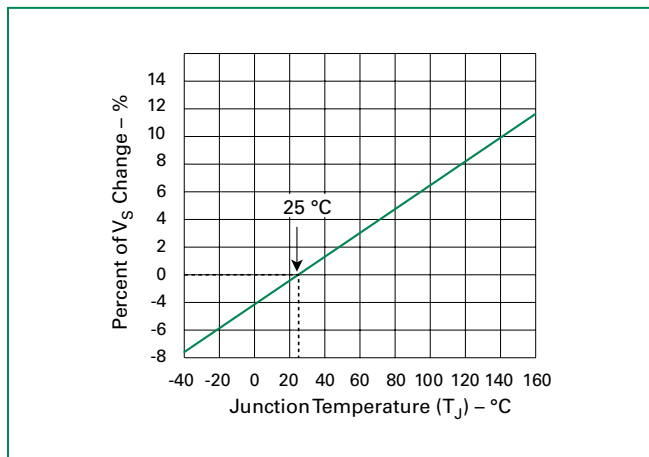
V-I Characteristics



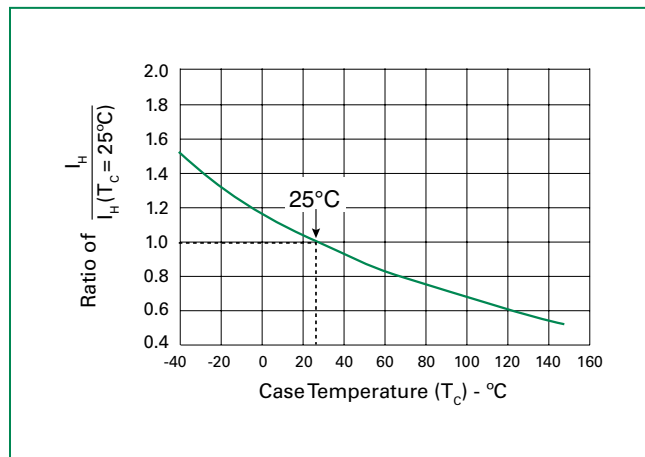
$t_r \times t_d$ Pulse Waveform



Normalized V_s Change vs. Junction Temperature

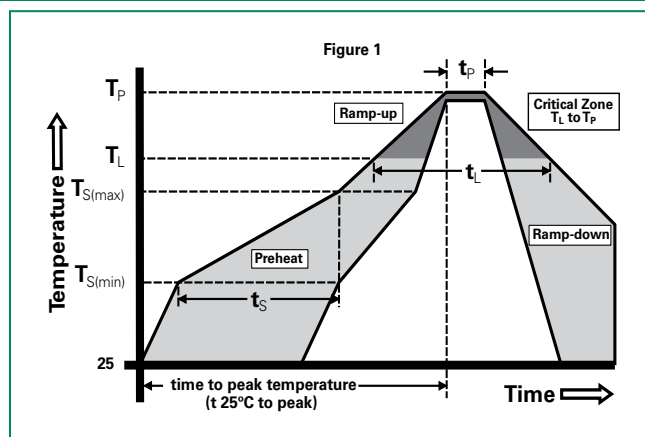


Normalized DC Holding Current vs. Case Temperature



Soldering Parameters

Reflow Condition	Pb-Free assembly (see Fig. 1)	
Pre Heat	-Temperature Min ($T_{s(\min)}$)	+150°C
	-Temperature Max ($T_{s(\max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)	3°C/sec. Max.	
$T_{s(\max)}$ to T_L - Ramp-up Rate	3°C/sec. Max.	
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_p)	+260(+0/-5)°C	
Time within 5°C of actual PeakTemp (t_p)	30 secs. Max.	
Ramp-down Rate	6°C/sec. Max.	
Time 25°C to Peak Temp (T_p)	8 min. Max.	
Do not exceed	+260°C	



Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL recognized epoxy meeting flammability classification V-0

Additional Information



Datasheet



Resources

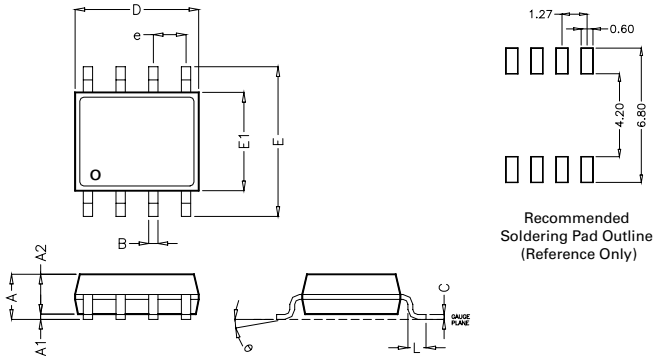


Samples

Environmental Specifications

High Temp Voltage Blocking	80% Rated $V_{DRM}(V_{DC}) + 125^\circ\text{C}$ or $+150^\circ\text{C}$, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to $+150^\circ\text{C}$, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	$52 V_{DC} (+85^\circ\text{C})$ 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	$+150^\circ\text{C}$ 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C , 1008 hrs.
Thermal Shock	0°C to $+100^\circ\text{C}$, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	$+121^\circ\text{C}$, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	$+260^\circ\text{C}$, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, $+85^\circ\text{C}$, 168 hrs., 3 reflow cycles ($+260^\circ\text{C}$ Peak). JEDEC-J-STD-020, Level 1

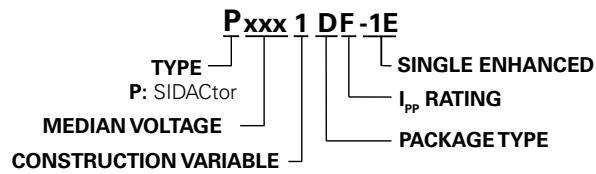
Dimensions — MS-012



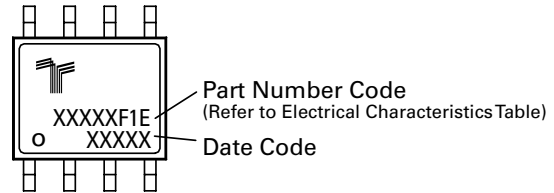
Dimension	Inches		Millimeters	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
A2	0.043	0.065	1.25	1.65
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.17	0.25
D	0.189	0.197	4.80	5.00
E	0.228	0.244	5.80	6.20
E1	0.150	0.157	3.80	4.00
e	0.050 BSC*		1.27 BSC*	
L	0.016	0.050	0.40	1.27

* BSC = Basic Spacing between Centers

Part Numbering



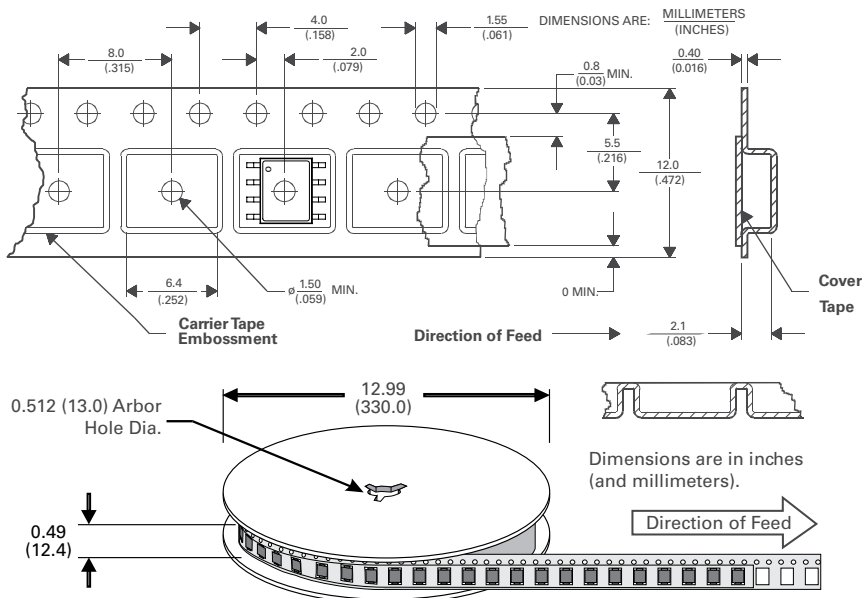
Part Marking



Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
D	MS-012 SMT 8-pin SOIC Tape and Reel Pack	2500	N/A	EIA-481-D

Tape and Reel Specifications — MS-012



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